Remarks

Applicant has amended the claims to overcome the Examiner's formal objections under 35 USC 112. Applicant's remarks on the Examiner's rejections over prior art follow.

The Examiner's rejection of all claims is premised upon the combination of the cache memory controller system of Cord et al. with the fault tolerant memory of Santeler et al. The Examiner reasons that a person of ordinary skill would have considered it obvious to combine what is described by Cord et al. and Santeler et al. by "modify[ing] the cache management system of Cord et al. to include the fault tolerant memory module system of Santeler et al., because then multiple memory module failures could be tolerated, system crashes prevented, and the swapping of memory modules included as taught by Santeler et al."

Applicant concurs with the Examiner's technical description of Cord et al. and Santeler et al., and will assume for the purposes of the rest of these remarks that there would be a motivation to combine Cord et al. and Santeler et al. for the purpose of tolerating failures, as the Examiner states. This acknowledged, however, Applicant disagrees with the Examiner's apparent conclusion that the combination of those two references would lead to the claimed invention. Rather, Applicant submits that a Cord et al. / Santeler et al. combination would clearly not lead to the invention claimed in this application.

Specifically, Applicant submits that the combination of Cord et al. and Santeler et al. would not include or lead to any feature or aspect in which the Cord et al. cache controller is made aware of changes in total hardware memory capacity so that, consistent with the recited step and function of the present claims, the controller can "respond[] to [the] change in [the] total usable hardware cache memory capacity for [the] DASD cache by altering [the] cache directory". Indeed, such a feature or aspect would be directly contrary to the intention and desires stated by Santeler et al. for his invention.

Santeler et al. has the clear purpose of creating a transparent "FAULT TOLERANT MEMORY", the key feature of which is stated at col. 4, lines 54-60:

The physical addressing performed by the memory controller 12 is transparent to the devices of the computer system 10. Thus, the mapping of data into the striped regions in the memory 11 is performed by the memory controller 12. As a result, preexisting software of the system 10 does not need to be modified, as the memory 11 appears to be one logical unit.

As this quotation makes clear, it is the essential purpose of Santeler et al. to provide a hardware RAID-striped memory that appears to other systems and software as one logical unit. That is, Santeler et al.'s goal is to implement fault-tolerant memory that a computer system can use in the same way it uses any other form of memory -- ignorant of the RAID features of

that memory, and assuming the memory is one logical unit that does not experience failures. Santeler et al.'s system is intended to be, and is, transparent to the rest of the system.

Applicant submits that a hypothetical combination of Cord et al. and Santeler et al., to be consistent with what is taught by both references, would involve using the Santeler et al. transparent RAID-striped memory to store data for the DASD cache described by Cord et al., thus improving the Cord et al. system by providing it a fault tolerant memory. Notably, however, the Cord et al. system would be unmodified -- it would use the DASD-striped memory of Santeler et al. the same way that it uses memory in its unmodified form described in US Patent 5,627,990 -- to store a cache directory and cache lines. The effect of Santeler et al.'s disclosure would be to store the directory and the cache lines redundantly in DASD-striped memory -- but the fact that memory is thus stored, would be unknown to the cache controller and not reflected in the cache directory. As a result, there would be no function in the combined system that would "respond[] to [the] change in [the] total usable hardware cache memory capacity for [the] DASD cache by altering [the] cache directory". Rather, consistent with Santeler et al., the system of Cord et al. would be insulated from, and unaware of, any changes in total usable hardware cache memory capacity, since the Santeler et al. RAID-striped memory would hide any such changes from the system of Cord et al.

Applicant notes the Examiner's observation that the process of "hot swapping" memory modules as is facilitated by Santeler et al., involves a "change in the total usable hardware memory". However, this does not mean that a Santeler et al. / Cord et al. combination would lead to the claimed invention. Indeed, the RAID scheme of Santeler et al. is exactly designed to prevent a "change in the total usable hardware memory" from being reflected or apparent in the total usable memory visible to the system. Rather, the RAID scheme of Santeler et al. intentionally includes redundant storage space so that the system can tolerate the loss of some amount of hardware memory without any change in the amount of memory visible to the system. Thus, to the contrary of the Examiner's position, Santeler et al. is clearly not about having a computer system react to changes in total usable hardware memory, but preventing the need for such reactions.

Applicant also notes the Examiner's observation that Santeler et al. must have some sort of directory or table to track the physical-to-physical memory mappings needed to implement a RAID scheme in multiple banks of memory. Assuming this is the case, it has no connection to the management of a cache directory. Specifically, Santeler's memory is not a cache; it may be used for cache storage, but if so, management of that cache would be done by software to which the Santeler et al. RAID

scheme is "transparent" and a "change in the total usable hardware memory" is hidden from view.

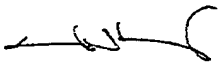
Applicant notes that the present invention is distinguishable from Santeler et al. combined with Cord et al., for reasons unique to the particular environment to which the invention is directed. Specifically, in the context of a read cache, Applicants observed that fault tolerant memory is not strictly required, for the reason that the data stored in a read cache is by definition a copy of data that is already stored in the DASD that it serves. Therefore, Applicants, rather than following the suggestions of Santeler et al. and adapting the memory for fault tolerance (so the memory never changes in visible capacity), instead adapted the read cache controller for fault tolerance, by programming it to respond to changes in visible capacity and accompanying losses of cached data, in a graceful manner. This unique environment, and the Applicant's unique approach to it, is neither disclosed nor suggested in the Santeler et al. or Cord et al. patents. It is a different and patentably unique approach in this specific environment.

All of the Examiner's rejections are premised on the combination of Cord et al. and Santeler et al. to arrive at the inventions of the independent claims, and thus all claims are allowable in view of the above remarks. While Applicant disagrees with the Examiner's use of other references in rejections of the dependent claims, for the purposes of brevity,

Applicant will limit these remarks to the independent claims and the combination of Cord et al. and Santeler et al., which remarks suffice, in Applicant's view, for allowance of the claims.

A petition for a three-month extension of time accompanies the transmittal of this communication. If, however, a petition is required, please consider this paper a petition for such an extension of time, and apply the appropriate extension of time fee to Deposit Account 23-3000. If any other charges or credits are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,



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